REMARKS

Claims 1-21 are all the claims presently pending in the application.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner objects to claim 21 for failure to reference back to a parent claim. Applicant believes the above claim amendment properly addresses the Examiner's concern and respectfully requests that the Examiner reconsider and withdraw this objection.

Claims 1-2, 8-9 and 15-16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kazuhiro (JP No. 11-097541). Claims 1-3, 7-10, 14-17 and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hathaway et al. (U.S. Patent No. 5,737,580). Claims 1-2, 4-9, 11-16 and 18-21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Fujine et al. (U.S. Patent No. 6,247,162 B1). Claims 1-2, 7-9, 14-16 and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nakamura (U.S. Patent No. 6,308,310 B1). Claims 1-21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Itazu et al. (U.S. Patent No. 6,405,354 B1).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention, as described in, for example, claim 1, is directed to a method for revising wiring of a circuit to prevent electro-migration. For each net in the circuit, each branch point in the net is identified, and a current density at each branch

point is calculated. It is then determined whether or not the current density exceeds a limit value and, if so, a wiring which affects the current density is revised in order to reduce the current density.

Conventional methods are not based on the concept of performing a current density analysis by first identifying the net branch points and then calculating the current density at that branch point.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Kazuhiro anticipates the present invention defined by claims 1, 2, 8, 9, 15, and 16. However, in spite of some arguable similarities, Applicant submits that the present invention is patentably distinguishable by reason of the plain meaning of the language of the independent claim. That is, Applicant submits that the present invention systematically checks the current density specifically by first locating the branch points of the nets in the circuit.

In contrast, the English Abstract of Kuzuhiro fails to suggest this specific technique and, instead, describes a technique in which "... the current density of all wires for connecting the function blocks ...." is calculated.

Applicant submits, that even if similar results are obtained, the present invention utilizes a patentably distinguishable technique of locating the net branch points for purpose of determining locations at which to calculate and compare current density.

The Examiner also alleges that Hathaway anticipates the present invention defined by claims 1-3, 7-10, 14-17, and 21.

Applicant submits, however, that even if there are arguably similarities with some aspects of the present invention, Hathaway is clearly patentably distinguishable. That is,

the description at lines 25-59 of column 5, upon which the Examiner relies, clearly describe a process that does not specifically rely upon identifying branch points for each net in the circuit.

The Examiner alleges that Fujine anticipates claims 1, 2, 4-9, 11-16, and 18-21.

Applicant submits, however, that, similar to the arguments above, the description at lines 7-10 of column 5, upon which the Examiner relies, applies only to the external power wiring, rather than the entire circuit, as in the claimed invention.

The Examiner also alleges that Nakamura anticipates claims 1, 2, 7-9, 14-16, and 21.

Applicant submits, however, that the description at lines 33-35 of column 2, upon which the Examiner relies, clearly states that the analysis therein is based upon the "path". This description, in combination with the description at lines 18-20 of column 5, indicates that the method of the present invention, in which each branching point is systematically identified and checked for current density, is clearly patentably distinguishable over Nakamura.

Finally, the Examiner also alleges that Itazu anticipates claims 1-21.

However, Applicant submits that the description at lines 7-12 of column 7, upon which the Examiner relies, does not teach or suggest using the net branch points as the location of the analysis, nor does it teach or suggest any part of the circuit except the power network portion.

Hence, turning to the clear language of the claims, in Kuzuhiro, Hathaway, Fujine, Nakamura, or Itazu, there is no teaching or suggestion for "... for each net in said circuit, identifying each branch point in said net; calculating a current density at each said branch point of said net....", as required by independent claim 1. The remaining independent

claims have similar language.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by any of these prior art references. Therefore, the Examiner is respectfully requested to withdraw these rejections.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-21, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 1/5/05

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FIG.4

WIRING PORTION	WIRING RESISTANCE [Ω]/CURRENT VALUE[A]
BETWEEN SOURCE OUTPUT TERMINAL (A) – WIRING CONNECTION POINT (B)	Rw1 = 30.0 / Iw1 = 10.0
BETWEEN WIRING CONNECTION POINT (B) – LOAD INPUT TERMINAL (C)	Rw2 = 30.0 / Iw2 = 10.0
BETWEEN WIRING CONNECTION POINT (B) – WIRING CONNECTION POINT (D)	Rw3 = 20.0 / Iw3 = 6.0
BETWEEN WIRING CONNECTION POINT (D) – LOAD INPUT TERMINAL (E)	Rw4 = 30.0 / Iw4 = 10.0
BETWEEN WIRING CONNECTION POINT (D) – WIRING CONNECTION POINT (F)	Rw5 = 40.0 / Iw5 = 15.0
BETWEEN WIRING CONNECTION POINT (F) – LOAD INPUT TERMINAL (G)	Rw6 = 30.0 / Iw6 = 10.0
BETWEEN WIRING CONNECTION POINT (F) – LOAD INPUT TERMINAL (H)	Rw7 = 40.0 / Iw7 = 15.0